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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,850	12/02/2003	Joel P. de Souza	YOR920030602US1 (17242)	3232

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,850	DE SOUZA ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *56,57 and 59-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *56, 57, and 59-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 06/052/2006 through 06/30/2006.

Claims 56, 57, and 59-79 are active in this application.

Claim(s) 1-55, 58, and 80 have been cancelled.

Remarks

2. Applicant's arguments filed 06/02/2006 have been fully considered, but are moot in view of new ground(s) of rejections.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim(s) 56, 57, and 59-79 is/are rejected under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent Application Publication No. 2004/0195646 by Yeo et al.

Regarding claim 56, Yeo discloses a planar hybrid-orientation semiconductor substrate structure, as shown in figs.1-4 and 9, comprising:

at least one clearly defined first single crystal semiconductor region 110 having a first surface crystal orientation <100> (see para. [0030-0031]), and

at least one clearly defined second single crystal semiconductor region 112 having a second surface crystal orientation <100> different from the first, said second single crystal semiconductor region 112 is formed by amorphizing a semiconductor material having said first orientation <100> and recrystallizing it into a semiconductor material having said second orientation <110> (see paras. [0040-0041] and claim 25), and said first single crystal semiconductor region 110 is laterally adjacent to said second single crystal semiconductor region 112 and both regions are disposed directly on a common buried insulating layer 114 that lays atop a substrate 116.

Nevertheless, the limitation(s) "said second semiconductor regions formed by amorphizing a semiconductor material having said first orientation and recrystallizing it into a semiconductor material having said second orientation" is process limitation(s), and the discussed claim is drawing to a product. The process limitation(s) of how the second semiconductor regions being formed has/have no patentable weight in claim drawn to structure. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also

In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue) and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. MPEP §2113 states that "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)."

Therefore, the recitation "said second semiconductor regions formed by amorphizing a semiconductor material having said first orientation and recrystallizing it into a semiconductor material having said second orientation" is considered a process of making product and is given no patentable weigtht in a product-by-process claim and is thus non-limiting.

Regarding claim 57, Yeo discloses the hybrid-orientation substrate structure further comprising at least one isolation region 118 separating said at least one first single crystal semiconductor region 110 from said at least one second single crystal semiconductor region 112. See figs. 1-2.

Regarding claim 59, Yeo discloses the planar hybrid-orientation substrate structure wherein said at least one isolation region comprises a dielectric-filled trench. See para. [0029].

Regarding claim 60, Yeo discloses the planar hybrid-orientation substrate structure wherein materials of said first and second semiconductor regions are selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloy thereof, and other III-V or II-VI compound semiconductors. See paras. [0039-0040].

Regarding claims 61-62, Yeo discloses the planar hybrid-orientation substrate structure comprising all claimed limitations. See paras. [0006] and [0039-0044].

Regarding claim 63, Yeo discloses the hybrid-orientation substrate structure wherein said different surface crystal orientations are selected from the group consisting of (110), (111) and (100). See paras. [0030].

Regarding claim 64, Yeo discloses the planar hybrid-orientation substrate structure wherein said first Si-containing semiconductor region 110 has a <100> crystal orientation and said second Si-containing semiconductor region 124 has a <110> crystal orientation. See para. [0031].

Regarding claim 65, Yeo discloses the planar hybrid-orientation substrate structure wherein one of said semiconductor regions has a (110) crystal orientation and said other semiconductor region has a (100) crystal orientation. See paras.[0030-0031].

Regarding claim 66, Yeo discloses the planar hybrid-orientation substrate structure further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a (100) crystal orientation and said at least pFET device is located on a (110) crystal orientation. See para. [0031].

Regarding claim 67, Yeo discloses the planar hybrid-orientation substrate structure further comprising at least one nFET device 122 and at least one pFET device 124, wherein said at least one nFET device 122 is located on a crystal orientation <100> that is optimal for said nFET device and wherein said at least pFET device 124 is located on a crystal orientation <110> that is optimal for said pFET device. See para. [0031].

Regarding claim 68, Yeo discloses the planar hybrid-orientation substrate structure wherein said buried insulator layer is a dielectric material selected from the group consisting of SiO_2, SiO_2 containing nitrogen, silicon nitride, metal oxides, metal nitrides, and highly thermally conductive materials. See para. [0036].

Regarding claim 69, Yeo discloses a planar hybrid-orientation semiconductor-on-insulator (SOI) substrate structure, as shown in figs. 5, comprising

at least one single-layer semiconductor region 110 (fig. 5f, where n-FET 122 being formed) comprising a semiconductor having a first single-crystal surface orientation <100> (see para. [0045-0046]), and

at least one bilayer semiconductor region 110&112 (fig. 5f, where p-FET 124 being formed) comprising a lower semiconductor layer 110 having said first single crystal surface orientation <100> and an upper semiconductor layer 112 having a second single crystal surface orientation <110> different from the first (see para. [0045-0046]), wherein said at least one single-layer semiconductor region 110 is laterally adjacent to said at least one bilayer semiconductor region 110&112 and both regions are disposed directly on a common buried insulating layer 114, said insulating layer 114 is located on a substrate 116.

Regarding claim 70, Yeo discloses the structure further including at least one isolation region separating said at least one single-layer semiconductor region from said at least one bilayer semiconductor region. See figs. 1, 5 and para. [0029].

Regarding claim 71, Yeo discloses the structure wherein said isolation region extends down at least to said common buried insulating layer. See figs. 1, 5.

Regarding claim 72, Yeo discloses the structure wherein said common buried insulator layer 114 is a dielectric material selected from the group consisting of SiO_2, SiO_2 containing nitrogen, silicon nitride, metal oxides, metal nitrides, and highly thermally conductive materials. See the specification, page 2-3 of the pending application. See para. [0036].

Regarding claim 73, Yeo discloses the planar hybrid-orientation substrate structure wherein said single-layer and bilayer semiconductor regions both comprise a semiconductor materials selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloy thereof, and other III-V or II-VI compound semiconductors. See paras. [0039-0040].

Regarding claims 74-75, Yeo discloses the planar hybrid-orientation SOI substrate structure comprising all claimed limitations. See paras. [0006] and [0039-0044].

Regarding claim 76, Yeo discloses the planar hybrid-orientation SOI substrate structure further comprising at least one nFET device 122 and at least one pFET

device124, wherein said at least one nFET device 122 is located on a crystal orientation <100> that is optimal for said nFET device and wherein said at least pFET device 124 is located on a crystal orientation <110> that is optimal for said pFET device. See para. [0031].

Regarding claim 77, Yeo discloses the hybrid-orientation SOI substrate structure wherein said different surface crystal orientations are selected from the group consisting of (110), (111) and (100). See paras. [0030].

Regarding claim 78, Yeo discloses the planar hybrid-orientation SIO substrate structure wherein one of said semiconductor regions (region 110) has a <100> crystal orientation and said other semiconductor region 112 has a <110> crystal orientation. See paras.[0030-0031].

Regarding claim 79, Yeo discloses the planar hybrid-orientation substrate structure further comprising at least one nFET device 122 and at least one pFET device 124, wherein said at least one nFET device 122 is located on a <100> crystal orientation and said at least pFET device 124 is located on a <110> crystal orientation. See para. [0031] and fig. 5f.

Conclusion

5. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571)272-1907. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

Douglas W. Owens 7/24/06

DOUGLAS W. OWENS
PRIMARY EXAMINER

Dao H. Nguyen
Art Unit 2818
July 21, 2006